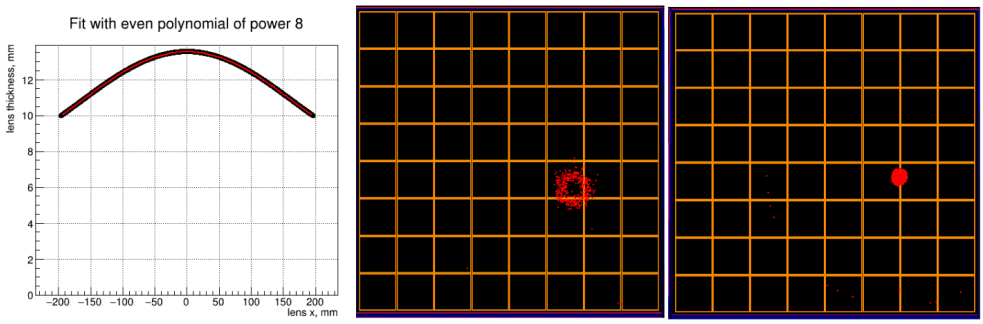

Figure 8: **Left:** The cross-section view of the corrector lens. **Center:** Photons induced by many UHECRs from 100 PeV protons, with equal parameters, superimposed on the camera plane. **Right:** PSF at the same location on the camera plane.

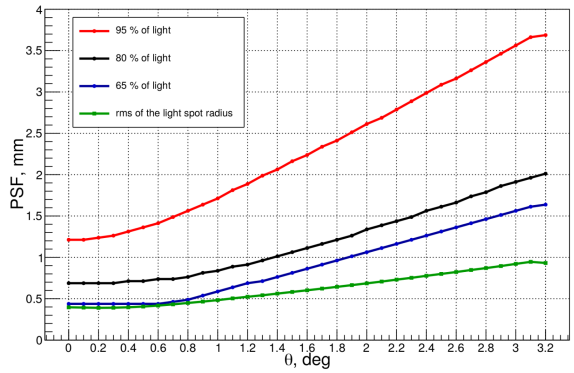

Figure 9: RMS of the radius of the light spot before (lower curve) and after (3 upper curves for different percentage of photon containment) it is processed by the optical elements of the telescope from Geant 4 simulation. For brevity we call this PSF on the y-axis.

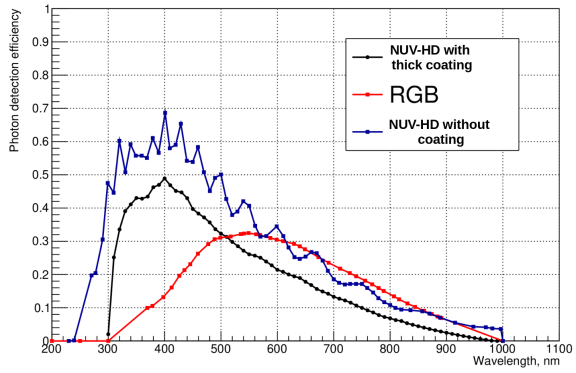

Figure 10: Photon detection efficiency versus photon wavelength for different SiPM types by FBK.

dominated by camera events when compared to telemetry data, we can derive the maximum event rate.

One event will have the size of:

$$\text{size}_{\text{event}} = \text{size}_{\text{event header}} + \text{N}_{\text{samples}} \times \text{ADC}_{\text{resolution}} \times \text{N}_{\text{pixels}} \quad (2)$$

where $\text{size}_{\text{event header}}$ = 34 bits (includes the bits dedicated to the alignment with the FPGA and and internal address of the readout units), $\text{N}_{\text{samples}}$ = 20, $\text{ADC}_{\text{resolution}}$ = 12 bit and the number of pixels, N_{pixels} = 9.

At a trigger rate of 240 Hz, the maximum data throughput for Terzina is reached. From simulations we derive the thresholds to obtain 120 Hz of the events with signal contained in a single pixel and 120 Hz with signal shared between two neighboring pixels.

Within this work, we consider 9 pixels pad to readout. However, at the beginning of the mission, we will read one ASIC or even a full camera for debugging/calibration purposes. Latter as soon we get our system fully understood we will shrink the redout pad, dropping all irrelevant information.

5.1 The trigger implementation

The ASIC offers the possibility of two programmable thresholds per channel hereinafter low and high threshold. The trigger will be structured so that, when the high threshold is passed by at least one channel, the waveforms of the 64 channels (one ASIC) are digitized and sent to the FPGA.

The time for the analog to digital conversion of all channels in the given ASIC, assuming the resolution of 12 bits takes 4096×5 ns, namely ~ 20.4μs. The digitised data readout time is 64 (channels) × 32 (time-cells) × 12 (resolution) × 1.25 ns (serialization in DDR) = 30.7 μs. Thus the total time for the analog to digital conversion and processing in the FPGA amounts to ~ 51.2 μs.

Considering a power-law increase in the number of UHECR events with a decreasing energy threshold, in order to avoid an obvious increase of the background, the low threshold trigger is defined using the coincidence of 2 adjacent pixels. The coincidence time window is chosen to be twice the rise time of the SiPM signal after amplification, namely τ = 20 ns (however this time window is configurable).

The implementation of the low level threshold trigger is the following: when at least two pixels cross the low threshold in one ASIC or in the 16 pixels along the edges of two neighboring ASICs within the coincidence window τ, a binary hit-map of the corresponding ASIC(s) is sent to the FPGA. The hit-map is analyzed to seek if there are at least two neighboring channels whose threshold is crossed